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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	MI22-1243
First Inventor or Application Identifier	Juengling
Title	Semiconductor Processing Methods of...
Express Mail Label No.	EL373342021

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [XX] * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing)
2. [XX] Specification [Total Pages 34] (plus title pg.) (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [XX] Drawing(s) (35 U.S.C. 113) [Total Sheets 12]
4. Oath or Declaration [Total Pages 3]
   a. [ ] Newly executed (original or copy)
   b. [XX] Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 17 completed) [Note Box 5 below]
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).
5. [XX] Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C.F.R.§3.73(b) Statement (when there is an assignee) [ ] Power of Attorney
10. [ ] English Translation Document (if applicable)
11. [XX] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [XX] Preliminary Amendment
13. [XX] Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. [ ] * Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. [XX] Other: Check #124225.

* A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:
[ ] Continuation [XX] Divisional [ ] Continuation-in-part (CIP) of prior application No: 09 / 036,701
Prior application information: Examiner Tsai Group / Art Unit: 2812

18. CORRESPONDENCE ADDRESS

[XX] Customer Number or Bar Code Label 021567 (Insert Customer No. or Attach bar code label here) or [ ] Correspondence address below

Name	David G. Latwesen, Ph.D.				
	WELLS, ST. JOHN, ROBERTS, GREGORY & MATKIN, P.S.				
Address	601 W. First Avenue, Suite 1300				
City	Spokane	State	WA	Zip Code	99201-3828
Country	USA	Telephone	(509) 624-4276	Fax	(509) 838-3424

Name (Print/Type)	David G. Latwesen, Ph.D.	Registration No. (Attorney/Agent)	38,533
Signature	[signature]	Date	10/21/99

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

<u>priority</u> Application Serial No. 09/036,701
<u>priority</u> Filing Date .... March 6, 1998
Inventor .... Werner Juengling
Assignee .... Micron Technology, Inc.
<u>priority</u> Group Art Unit 2812
<u>priority</u> Examiner .... H. Tsai
Attorney's Docket No. MI22-1243
Title: Semiconductor Processing Methods of Forming Devices on a Substrate, Forming Device Arrays on a Substrate, Forming Conductive Lines on a Substrate, and Forming Capacitor Arrays on a Substrate, and Integrated Circuitry

PRELIMINARY AMENDMENT

To: BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

From: David G. Latwesen (Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

AMENDMENTS

In the Specification

At p. 1 before the "Technical Field" section, please insert the following:

--**RELATED PATENT DATA**

This patent resulted from a divisional application of U.S. Patent Application Serial No. 09/036,701, filed March 6, 1998, which is a

divisional application of U.S. Patent Application Serial No. 08/742,895, filed November 1, 1996.--

In the Claims:

Cancel claims 1-50.

New Claims

51. A method of forming a plurality of DRAM capacitors comprising:

etching capacitor container openings for an array in a substrate in at least two separate etching steps, and forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps.

52. The method of claim 51 wherein the forming electrically insulative partitions step comprises:

forming insulative material over the substrate; and

conducting an anisotropic etch of the insulative material to a degree sufficient to leave the partitions.

53. A processing method of forming a plurality of DRAM capacitors comprising etching capacitor container openings for a capacitor array in a substrate in two separate etching steps.

REMARKS

Claims 1-50 are canceled and new claims 51-53 are added. Claims 51-53 correspond to claims 56-58 of the parent application, which an Examiner of the parent application indicated pertain to a distinct species relative to other claims of the priority application. Applicant requests examination of claims 51-53.

Respectfully submitted,

Dated: 10/21/99

By: [signature]

David G. Latwesen, Ph.D.
Reg. No. 38,533

EL373342021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Semiconductor Processing Methods Of Forming Devices On A Substrate, Forming Device Arrays On A Substrate, Forming Conductive Lines On A Substrate, And Forming Capacitor Arrays On A Substrate, And Integrated Circuitry

* * * * *

INVENTOR

Werner Juengling

ATTORNEY'S DOCKET NO. MI22-483

EM156306369

EM057275136

TECHNICAL FIELD

This invention relates to semiconductor processing methods of forming devices on or over a substrate, forming device arrays on or over a substrate, forming conductive lines on or over a substrate, and forming capacitor arrays on or over a substrate. The invention also relates to semiconductor device arrays, and in particular to series of conductive lines and capacitor arrays.

BACKGROUND OF THE INVENTION

Circuit devices which are fabricated on or over semiconductor wafers typically undergo one or more photolithographic steps during formation. During such photolithographic steps, device features can be etched using conventional techniques. The spacing between such devices is important because often times adjacent devices must be electrically isolated from one another to avoid undesirable shorting conditions.

One of the limitations on device spacing stems from limitations inherent in the photolithographic process itself. In the prior art, devices are generally spaced only as close as the photolithographic limit will permit.

By way of example and referring to Figs. 1 and 2, a semiconductor wafer fragment is indicated generally by reference numeral 25. Fragment 25 includes a substrate 29 atop which a material 28 is provided. A plurality of patterned masking layers 26 are formed atop material 28.

Referring to Fig. 3, material 28 is anisotropically etched to form lines 30 atop substrate 29. As shown, individual lines have respective widths L_1 which constitute the minimum photolithographic feature size available for a line. Typically, a separation S_1 separates adjacent lines across the substrate as shown. Such dimension is typically only slightly larger than L_1 but could be the same as L_1. The term "pitch" as used in this document is intended to be in its conventional usage, and is defined as the distance between one edge of a device and the corresponding same edge of the next adjacent device. Accordingly and in the illustrated example, the pitch between adjacent lines P_1 (i.e., from the left illustrated edge of one line to the left illustrated edge of the next immediately adjacent line) is equal to the sum of L_1 and S_1.

As integrated circuitry gets smaller and denser, the need to reduce spacing dimensions or pitch, such as S_1 and P_1, becomes increasingly important. This invention grew out of the need to reduce the size of integrated circuits, and particularly the need to reduce spacing dimensions and pitches between adjacent devices over a semiconductor wafer.

SUMMARY OF THE INVENTION

The invention includes semiconductor processing methods and related integrated circuitry in which a plurality of patterned device outlines are formed over a semiconductor substrate. Electrically insulative partitions or spacers are then formed on at least a portion

of the patterned device outlines, after which a plurality of substantially identically shaped devices are formed relative to the patterned device outlines. Individual formed devices are spaced from at least one other of the devices by a distance substantially no more than a width of one of the electrically insulative spacers.

According to one aspect of the invention, elongated electrically conductive lines are formed. According to another aspect of the invention, capacitors are formed. In one preferred implementation of the latter aspect, a pair of adjacent capacitor containers are formed over a substrate by etching a first capacitor container opening having at least one sidewall. An electrically insulative spacer is formed over the sidewall. A second capacitor container opening is etched selectively relative to the spacer. Capacitors are then formed in the capacitor containers in a manner such that adjacent capacitors have a separation distance which is substantially no greater than the width of the spacer between the adjacent capacitors.

A novel masking layout is provided which allows capacitors to be formed in a manner which reduces device pitch by almost 50%. Such is particularly adaptive for use in fabrication of DRAM circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a top plan view of a prior art semiconductor wafer fragment atop which a plurality of masking layers are formed, and is discussed in the "Background" section above.

Fig. 2 is a side sectional view of the Fig. 1 prior art semiconductor wafer taken along line 2-2 in Fig. 1.

Fig. 3 is a view of the Fig. 1 prior art semiconductor wafer fragment at a processing step subsequent to that shown in Fig. 1.

Fig. 4 is a top plan view of a semiconductor wafer fragment atop which a plurality of masking layers are formed at one processing step in accordance with one aspect of the invention.

Fig. 5 is a side view of the Fig. 4 semiconductor wafer fragment.

Fig. 6 is a view of the Fig. 5 semiconductor wafer fragment at a processing step subsequent to that shown by Fig. 5.

Fig. 7 is a view of the Fig. 5 semiconductor wafer fragment at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a view of the Fig. 5 semiconductor wafer fragment at a processing step subsequent to that shown by Fig. 7.

Fig. 9 is a view of the Fig. 5 semiconductor wafer fragment at a processing step subsequent to that shown by Fig. 8.

Fig. 10 is a top plan view of the Fig. 9 semiconductor wafer fragment.

Fig. 11 is a view of a semiconductor wafer fragment at one processing step in accordance with another aspect of the invention.

Fig. 12 is a view of the Fig. 11 semiconductor wafer fragment at a processing step subsequent to that shown by Fig. 11.

Fig. 13 is a view of the Fig. 11 semiconductor wafer fragment at a processing step subsequent to that shown by Fig. 12.

Fig. 14 is a view of the Fig. 11 semiconductor wafer fragment at a processing step subsequent to that shown by Fig. 13.

Fig. 15 is a view of the Fig. 11 semiconductor wafer fragment at a processing step subsequent to that shown by Fig. 14.

Fig. 16 is a view of the Fig. 11 semiconductor wafer fragment at a processing step subsequent to that shown by Fig. 15.

Fig. 17 is a view of the Fig. 11 semiconductor wafer fragment at a processing step subsequent to that shown by Fig. 16.

Fig. 18 is a view of the Fig. 11 semiconductor wafer fragment at a processing step subsequent to that shown by Fig. 17.

Fig. 19 is a top plan view of a portion of a semiconductor mask layout in accordance with one aspect of the invention.

Fig. 20 is a top plan view of the Fig. 19 semiconductor mask layout with a portion highlighted for purposes of discussion.

Fig. 21 is a view of a portion of the Fig. 20 semiconductor mask layout highlighted portion.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring initially to Figs. 4 and 5, a plurality of patterned device outlines 32 are photolithographically formed over a semiconductive substrate 34. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. In this illustrated and preferred example, the material constituting outlines 32 is preferably of the type which can be etched selectively relative to substrate 34. Such outlines define areas over substrate 34 in which conductive lines are to be formed. Such patterned device outlines are, dimension-wise, substantially the same as those set forth with regard to patterned masking layers 26 in Figs. 1-3.

Referring to Fig. 6, an electrically insulative material such as SiO_2 or Si_3N_4 is formed over lines 32 and substrate 34 and subsequently anisotropically etched to provide a plurality of sidewall spacers 36 on at least a portion, and preferably all, of pattern device outlines 32. For purposes of the ongoing discussion, patterned device outlines 32 define male patterns between which female patterns 38 are also formed. Accordingly, an array of alternating male/female patterns are formed

over the substrate wherein sidewall spacers 36 are formed in female patterns 38.

Referring to Fig. 7, and after forming sidewall spacers 36, male patterns or patterned device outlines 32 are removed as by suitable etching techniques. The etch preferably etches device outlines 32 relative to the material forming spacers 36 and the substrate 34. Such leaves behind a plurality of upstanding sidewall spacers 36 which effectively define thin electrically insulative partitions between which a plurality of devices are to be formed. As shown, the distance or lateral spacing between adjacent spacers varies from spacer-to-spacer. According to one preferred aspect, a plurality of spaces 40a through 40i are provided wherein adjacent spaces, such as 40a and 40b differ slightly in lateral width dimension, while alternate spaces such as 40a and 40c have as shown substantially the same lateral width dimension.

Referring to Fig. 8, a conductive material 42 is formed over substrate 34 and sidewall spacers 36 and preferably completely fills spaces 40a through 40i. An example material for layer 32 is conductively doped polysilicon.

Referring to Fig. 9, conductive material 42 is etched back as by suitable methods such as a chemical-mechanical polish (CMP) or dry etching as well known in the art. Such forms a plurality of substantially identically shaped circuit devices relative to the patterned device outlines 32 (Fig. 6). In this embodiment, such devices are conductive lines 44 which are spaced laterally from one another a

distance which is no greater than a width of one of the electrically insulative sidewall spacers 36 therebetween. As so formed, immediately adjacent conductive lines of the plurality of lines formed have a pitch P_2 which is substantially no greater than a lateral line width L_2 plus a width W_2 of the spacer 36 which is positioned between the adjacent lines. As compared to the pitch P_1 (Fig. 3) of the prior circuit devices, pitch P_2 represents a reduction in pitch which approaches fifty percent. Such achieved pitch reductions are without regard to the prior art photolithographic spacing constraints imposed on semiconductor processing. As mentioned above, the spacing between adjacent spacers varies from spacer-to-spacer. Accordingly, the pitch P_2 would vary as well. It is possible for the spacing between adjacent spacers to be uniform, however, so that the pitch remains constant across the substrate.

Referring to Fig. 10, a top plan view of substrate 34 is shown. Conductive lines 44 collectively define a series of conductive lines which in turn define a device array 46 of substantially identically shaped devices. Array 46 includes the plurality of upstanding spacers 36 and the conductive lines 44 formed intermediate the spacers. In accordance with a preferred aspect of the invention and as described with reference to Fig. 9 above, adjacent lines have a pitch which is substantially no greater than about the distance between a pair of adjacent spacers (corresponding to the line width) plus the width of the spacer therebetween. In the illustrated example, conductive lines 44 are

elongated and adjacent conductive lines have different lateral line widths. Additionally, alternate lines have substantially equal lateral line widths. Such variation in line width stems from the manner in which the anisotropically etched sidewall spacers 36 are provided over the substrate, and in particular the lateral spacing of device outlines 32 (Fig. 5). As mentioned above, it is possible for the line widths to be substantially equal over the entire substrate.

Referring still to Fig. 10, a dashed line 48 traverses device array 46. Individual elongated conductive lines 44 are formed over substrate 34 transversely along line 48. Respective alternate devices along line 48 have a substantially common width dimension therealong and respective adjacent devices have a different width dimension therealong.

Referring collectively to Figs. 11-18, a semiconductor processing method of forming a plurality of alternate devices on a substrate in accordance with the above-described principles is described. According to a preferred aspect of the invention, the devices comprise capacitors, and even more preferably comprise capacitors which form part of a dynamic random access memory (DRAM) device. Circuit devices other than the illustrated and described conductive lines and capacitors can be fabricated in accordance with the invention.

In accordance with one preferred embodiment, a plurality of capacitor container openings are etched over a substrate in two separate etching steps. Thereafter, corresponding DRAM capacitors are formed

within the container openings according to known processing techniques. As so formed, and in accordance with the above-described spacer formation and pitch reduction concepts, a plurality of pairs of adjacent capacitors are formed in respective adjacent capacitor containers which are separated by no more than anisotropically etched, electrically insulative sidewall spacers as will become evident below.

Referring specifically to Fig. 11, a semiconductor wafer fragment in process is shown generally at 50 and includes a layer of material 52 which may or not may be semiconductive. Transistors forming part of the preferred DRAM circuitry array are not shown, but are formed preferably elevationally below the capacitors described hereafter. Other elevational configurations as between transistors and capacitors are possible. A layer 54, preferably of borophosphosilicate glass (BPSG), is formed over material 52 to a thickness preferably around two microns. A layer of photoresist material 58 formed over the substrate and patterned to define a plurality of bit line contact openings 56 over wafer fragment 50. The illustrated and preferred photoresist material 58 defines a plurality of patterned device outlines 60 over the substrate. Patterned outlines 60 in turn define individual areas over the substrate for supporting a plurality of capacitors to be formed as described below. Preferably, the individual areas defined by outlines 60 support two such capacitors as will be apparent.

Referring to Fig. 12, layer 54 is anisotropically etched to form bit line contact openings 62 into layer 54. Photoresist material 58 is then

stripped and an insulating material is formed over the substrate and into openings 62 and subsequently anisotropically etched to form the illustrated sidewall spacers 64. Thereafter, bit contact material, preferably conductively doped polysilicon, is formed over the substrate and into openings 62. Such material is or may be planarized as by suitable chemical-mechanical polishing to provide the illustrated bit line contacts or plugs 66. A plurality of contacts similar to contacts 66 are formed over the substrate during the same formation steps and bound each area 60 across the substrate in the same manner as the illustrated contacts 66 bound the centermost area 60.

Referring to Fig. 13, a first set of capacitor container opening patterns 68 are formed over the substrate and defined by photoresist material 69. The device pattern set forth in Fig. 13 results from a semiconductor mask layout which is shown in Fig. 19 and discussed in detail below. Fig. 13 is a view which is taken along line 13-13 in Fig. 19.

Referring to Fig. 14, a first set 70 of capacitor container openings are etched selectively relative to spacers 64 and the conductive contacts 66 through layer 54. Photoresist material 69 is then stripped away. Individual capacitor containers 72 of first set 70 have at least one, and preferably more, upright sidewalls, two of which are illustrated at 74, 76 respectively for each container 72. Upright sidewalls 74 as viewed in Fig. 14 coincide with and are defined by the rightmost sidewall spacer 64 which was previously formed.

Referring to Fig. 15, an electrically insulative material such as silicon nitride is formed over the substrate and subsequently anisotropically etched relative to layer 54, spacers 64, and bit line contacts 66 to form respective partitions or spacers 78, 80. Individual areas defined by outlines 60 are thus partitioned into two parts which are separated from one another by non-conducting partitions 78, 80, respectively, which are formed over and cover sidewalls 74, 76 respectively. As so formed, partitions 78, 80 outline individual container openings of first set 70 in which capacitors are to be formed.

Referring to Fig. 16, remaining BPSG layer 54 is selectively etched or otherwise removed relative to sidewall spacers 64, spacers or partitions 78, 80, and bit line contacts 66 to define a second set 82 of capacitor container openings to respective capacitor containers 84. As so etched, individual second set containers 84 and the respective openings thereof are disposed adjacent respective first set containers 72 to form a pair of containers (only one complete pair 72/84 of which is shown). The leftmost side of Fig. 16 shows a leftmost outline 60 which includes a complete capacitor container 84 and a portion of its paired container 72. Likewise, the rightmost side of Fig. 16 shows a rightmost outline 60 which includes a complete capacitor container 72 and a portion of its paired container 84. Individual containers of a pair are separated therefrom by no more than the width of a non-conducting partition 80. As discussed above with reference to the pitch advantages achieved with conductive lines 44 (Figs. 9 and 10),

such advantages are achieved through the use of spacers or partitions 80 which electrically isolate adjacent capacitors formed in respective areas 60.

Referring to Figs. 17 and 18, electrically conductive container material 86 is formed over the substrate and planarized (Fig. 18) to define a plurality of capacitor storage nodes 81 in preferred container shapes. Subsequently, capacitors are formed according to conventional formation techniques as by provision of a dielectric layer 83 over respective storage nodes 81 and provision of a subsequent polysilicon layer 85 thereover. As so formed, capacitors in respective partitioned parts of the area defined by outlines 60 are separated from immediately adjacent capacitors or have a closest separation distance which is substantially no greater than the width of the partition or spacer between the capacitors.

Referring to Fig. 19, a diagrammatic semiconductor mask layout and DRAM array is designated generally by reference numeral 88. Layout 88 is utilized to enable the above-described container openings to be selectively, alternately formed or etched in the two described separate etching steps. For purposes of clarity, Fig. 13 is taken along line 13-13 in Fig. 19 at a processing point just after the patterning of photoresist material 69 (Fig. 13) with layout 88. Layout 88 enables capacitors having unique, space-saving geometries to be formed over the substrate. According to a preferred aspect of the invention, the electrically insulative partitions 78, 80 (Fig. 16) are formed between

adjacent capacitors intermediate the two etching steps which form or define the areas over the substrate in which the capacitors will be formed. The partitions 78, 80 are not shown for clarity in Fig. 19.

Mask layout 88 includes a plurality of rows such as those illustrated at R_1, R_2, R_3, and R_4. The mask layout also includes a plurality of columns such as those illustrated at C_1, C_2, C_3, C_4, C_5, C_6, and C_7. A plurality of masked areas 90 and a plurality of adjacent unmasked areas 92 are defined by the layout. Unmasked areas 92 correspond to capacitor container opening patterns 68 in Fig. 13 and masked areas 90 correspond to photoresist material 69. Layout 88 enables a plurality of capacitors to be formed, preferably as part of a DRAM array over the substrate, wherein respective alternate capacitors in a row, such as rows R_1-R_4 have substantially similar lateral width profiles transverse the row. Preferably, respective adjacent capacitors in a row have different lateral width profiles transverse the row. The illustrated and preferred lateral width profiles when viewed from a point above the substrate approximate triangles which are oriented in a top-to-bottom fashion across the row. Additionally, individual defined areas in which the preferred capacitor pairs are to be formed (corresponding to the view taken along line 13-13 in column C_5) approximate a diamond shape with such shape having at its respective corners, bit line contacts 94 which are formed as described above. For purposes of the ongoing discussion, each of columns C_1-C_7 are formed along a generally straight line which is generally transverse each of rows R_1-R_4. Further,

the array of capacitor pairs to be formed are formed along individual lines which contain at least one of the pairs of capacitors. As such, the array is defined by a plurality of the lines (corresponding to the plurality of the columns) which contain a plurality of capacitors which are separated by substantially no more than an electrically insulative anisotropically etched spacer as described above. Underlying word lines are shown by dashed lines 93 and interconnect associated transistors formed relative to the substrate. Individual bit lines are not specifically shown but are subsequently formed and oriented generally transversely relative to word lines 93.

Referring to Fig. 20, mask layout 88 defines in part a DRAM array which includes a plurality of six-capacitor geometries which are to be formed over the substrate. A representative of one of the geometries is indicated generally by reference numeral 96 and a plurality of adjacent or other geometries are shown in phantom lines. The illustrated and preferred six-capacitor geometries are, in turn, defined by a plurality of individual polygonal capacitor geometries shown collectively at 98 through 108. Preferably, collective individual capacitor geometries 98 through 108 approximate a hexagon individual sides of which are defined by a side of a different respective one of the individual polygonal capacitor geometries. For example, six-capacitor geometry or hexagon 96 includes six sides collectively shown at 96a, 96b, 96c, 96d, 96e, and 96f. Each of such sides is defined by a different respective one of the individual sides of the individual

polygonal capacitor geometries 98 through 108. According to a preferred aspect of the invention, individual polygonal capacitor geometries 98 through 108, when viewed outwardly of the substrate approximate a wedge or wedge-shape. Even more preferably, such individual geometries approximate a triangle which, most preferably, is an isosceles triangle. Further, individual approximated isosceles triangles include equal adjacent angles θ which approximate a range of between about 50° to 70°. Such equal adjacent angles are shown for individual geometries 100, 104, and 108. Even more preferably, such equal adjacent angles approximate an angle of about 65°. Individual geometries 98 through 102 and 104 through 108 respectively, are preferably arranged in a top-to-bottom orientation such that hexagon 96 can be bisected, as by dashed line 110, into halves which contain exactly three individual polygonal capacitor geometries. In the illustrated and preferred hexagon, one of the halves, a top half as viewed in Fig. 20 contains individual geometries 98, 100, and 102. The other of the halves, a bottom half, contains geometries 104, 106, and 108.

Referring to Fig. 21, the top half containing geometries 98, 100, and 102 is shown. Such comprises a three-capacitor geometry 112, a plurality of which are disposed over the substrate. Preferably, three-capacitor geometry 112, when viewed outwardly of the substrate defines a pair of overlapping approximated parallelograms, the intersection of which approximates a triangle. The first of such parallelograms is shown at 114. The second of such parallelograms is

shown at 116. Parallelogram 114 includes sides 114a, 114b, 114c, and 114d. Parallelogram 116 includes sides 116a, 116b, 116c, and 116d. The parallelograms share sides 114b and 116d. As shown, each approximated parallelogram is bounded at a respective one of its corners by a bit line contact 94. The approximated triangle defined by the intersection of parallelograms 114, 116 includes sides 114c, 116c and shared sides 114b/116d. For purposes of ongoing discussion, a plurality of capacitor pairs are selectively and alternately etched over the substrate along etch axes which are generally orthogonal relative to the substrate and into the plane of the page upon which Fig. 21 appears. Such capacitor pairs can approximate the above described parallelogram and would include the individual capacitors etched as a result of individual geometries 98, 100, or alternatively 100, 102.

Referring to both Figs. 16 and 19, a DRAM array is formed atop a substrate and includes a first set of capacitors formed in first set capacitor openings 70 over the substrate. A second set of capacitors are formed over the substrate and in second set capacitor openings 82. Individual capacitors of the first set are bounded by at least three capacitors from the second set (Fig. 19). Preferably, individual first set capacitors have a closest separation distance from at least one of the three bounding capacitors which is substantially no more than a width of an electrically insulative anisotropically etched spacer. One such width is indicated in Fig. 16 at 80. Even more preferably, individual bounded first set capacitors have closest separation distances from no

less than two and preferably three of the bounding capacitors which are no more than the width of an electrically insulative anisotropically etched spacer formed or provided between the respective capacitors.

The above described semiconductor device forming methods and integrated circuitry formed thereby constitute an improvement which relates to device spacing over a substrate. Such improvement enables device pitch to be reduced by almost fifty percent or more which represents a substantial space savings over heretofore available methods and devices.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method of forming integrated circuit devices comprising:

forming a plurality of patterned device outlines over a semiconductive substrate;

forming electrically insulative spacers on at least a portion of the patterned device outlines; and

forming a plurality of substantially identically shaped devices relative to the patterned device outlines, at least two individual devices of the plurality being spaced from one another by a distance no greater than a width of an interposed electrically insulative spacer.

2. The method of forming integrated circuit devices of claim 1, wherein the devices are elongated electrically conductive lines.

3. The method of forming integrated circuit devices of claim 1, wherein the devices include capacitors of a DRAM array.

4. The method of forming integrated circuit devices of claim 1, wherein the plurality of devices are formed along a line, respective alternate devices along the line having a substantially common width dimension.

5. The method of forming integrated circuit devices of claim 1, wherein the plurality of devices are formed along a line, respective adjacent devices along the line having different width dimensions.

6. The method of forming integrated circuit devices of claim 1, wherein the devices include capacitors of a DRAM array, the capacitors being formed in rows, respective alternate capacitors in a row having substantially similar width profiles transverse the row.

7. The method of forming integrated circuit devices of claim 1, wherein the devices include capacitors of a DRAM array, the capacitors being formed in rows, adjacent capacitors in a row having different width profiles transverse the row.

8. The method of forming integrated circuit devices of claim 1, wherein the devices include capacitors of a DRAM array, the capacitors being formed in rows, respective alternate capacitors in a row having substantially similar width profiles transverse the row, adjacent capacitors in the row having different width profiles transverse the row.

9. A method of forming a plurality of integrated circuitry devices on a substrate comprising:

forming a plurality of spaced, upstanding, anisotropically etched electrically insulative spacers; and

forming a plurality of devices over the substrate intermediate the spacers with the spacers being positioned intermediate adjacent devices, adjacent devices having a pitch which is substantially no greater than about the distance between a pair of adjacent spacers plus the width of the spacer between the adjacent devices.

10. The method of forming a plurality of integrated circuitry devices of claim 9, wherein the devices are conductive lines.

11. The method of forming a plurality of integrated circuitry devices of claim 9, wherein the devices are capacitors.

12. The method of forming a plurality of integrated circuitry devices of claim 9, wherein the devices are capacitors of a DRAM device.

13. A DRAM capacitor forming method comprising the steps of:

forming a plurality of patterned outlines over a semiconductive substrate to define individual areas for a plurality of capacitors to be formed;

partitioning said individual areas from one another by a non-conducting partition; and

forming capacitors in at least some of the respective partitioned areas, the respective capacitors being separated from immediately adjacent capacitors by a distance substantially no greater than the width of the partition therebetween.

14. The DRAM capacitor forming method of claim 13, wherein the partitioning step comprises:

etching a first set of capacitor container openings, individual container openings having at least one upright sidewall; and

etching a second set of capacitor container openings adjacent respective first set container openings and separated therefrom by respective non-conducting partitions.

15. The DRAM capacitor forming method of claim 13, wherein the partitioning step comprises:

etching a first set of capacitor container openings, individual container openings having at least one upright sidewall;

forming insulative material over the substrate;

anisotropically etching the insulative material to provide partitions over at least some of the upright sidewalls; and

etching a second set of capacitor container openings immediately adjacent the provided partitions.

16. The DRAM capacitor forming method of claim 13 wherein individual defined areas, when viewed from a point above the substrate, approximate diamond shapes.

17. A DRAM capacitor forming method comprising the steps of:

forming a pair of adjacent capacitor containers over a substrate by etching a first capacitor container opening having at least one upright sidewall;

forming an electrically insulative spacer on the upright sidewall;

selectively etching a second capacitor container opening adjacent the formed spacer;

forming capacitors in the capacitor containers, adjacent capacitors having a separation distance therebetween which is substantially no greater than the width of the spacer between the adjacent capacitors.

18. The DRAM capacitor forming method of claim 17, wherein the step of forming the electrically insulative spacer comprises:

forming an insulative material over the substrate; and

anisotropically etching the insulative material to form the spacer.

19. The DRAM capacitor forming method of claim 17, wherein individual capacitor containers are generally triangularly shaped when viewed from a point above the substrate.

20. A method of forming capacitors comprising forming an array of capacitor pairs on a substrate, the array being defined in part by a plurality of lines, individual lines containing at least one pair of capacitors, individual capacitors of said at least one pair of capacitors being separated by substantially no more than an electrically insulative anisotropically etched spacer disposed therebetween.

21. The method of forming capacitors of claim 20 further comprising prior to forming the array of capacitor pairs, forming a plurality of bit line contacts in individual lines, individual capacitor pairs being bounded by at least two bit line contacts.

22. The method of forming capacitors of claim 20 wherein individual capacitor pairs have a pitch no greater than about a lateral width dimension of one of the capacitors plus the width of the anisotropically etched spacer between the capacitors of an individual pair.

23. A DRAM capacitor array comprising:

a substrate;

a first set of capacitors over the substrate; and

a second set of capacitors over the substrate, individual capacitors of the first set being bounded by at least three capacitors from the second set, individual first set capacitors having a closest separation distance from at least one of the three capacitors from the second set which is substantially no more than a width of an interposed electrically insulative anisotropically etched spacer.

24. The DRAM capacitor array of claim 23, wherein individual bounded first set capacitors have closest separation distances from no less than two of the three capacitors from the second set, said closest separation distances being substantially no more than a width of an interposed electrically insulative anisotropically etched spacer.

25. The DRAM capacitor array of claim 23. wherein individual bounded first set capacitors have closest separation distances from the three capacitors from the second set which are substantially no more than a width of an interposed electrically insulative anisotropically etched spacer.

26. A method of forming a plurality of capacitors in a semiconductor memory device comprising the steps of:

selectively removing substrate material to define a first set of containers;

forming sidewall spacers adjacent container sidewalls;

selectively removing remaining substrate material adjacent the spacers to define a second set of containers; and

forming capacitors in the containers separated only by the spacers.

27. The method of forming a plurality of capacitors of claim 26 further comprising prior to defining the first set of containers:

forming a plurality of bit line contact openings over the substrate, individual bit line contact openings having at least one sidewall; and

covering the at least one sidewall of the plurality of bit line contact openings with an insulating material.

28. The method of forming a plurality of capacitors of claim 26 further comprising prior to defining the first set of containers:

forming a plurality of bit line contact openings over the substrate, individual bit line contact openings having at least one sidewall;

covering the at least one sidewall of the plurality of bit line contact openings with an insulating material;

etching the insulating material to form sidewall spacers; and

forming electrically conductive material in the bit line contact openings to provide bit line contacts,

wherein the defining of the first set of containers includes selectively etching the first set of containers relative to the sidewall spacers and the electrically conductive material of the bit line contacts.

29. A DRAM capacitor forming method comprising forming a plurality of pairs of adjacent capacitors in respective adjacent capacitor containers separated by substantially no more than anisotropically etched sidewall spacers.

30. The DRAM capacitor forming method of claim 29, wherein individual pairs of adjacent capacitors, when viewed from a point over the substrate are approximately diamond shaped.

31. The DRAM capacitor forming method of claim 29 further comprising forming a plurality of bit line contact openings over the substrate prior to forming the capacitor pairs.

32. The DRAM capacitor forming method of claim 29 further comprising forming a plurality of bit line contact openings over the substrate prior to forming the capacitor pairs, and wherein individual pairs of adjacent capacitors, when viewed from a point over the substrate are approximately diamond shaped, individual bit line contact openings being positioned in respective corners of the diamonds.

33. A capacitor array for a DRAM comprising:

a plurality of bit line contacts to a substrate; and

a plurality of capacitor pairs selectively alternately etched over a substrate along etch axes which are generally orthogonal relative to the substrate, individual capacitor pairs having an area which, when viewed from outwardly of the substrate from a point on such etch axes, approximates a parallelogram which is bounded at a plurality of its corners by individual bit line contacts.

34. A processing method of forming a capacitor array for a DRAM comprising:

forming a plurality of bit line contacts to a substrate; and

forming a plurality of capacitor pairs, individual pairs being selectively alternately etched over a substrate and along etch axes which are generally orthogonal relative to the substrate, individual capacitor pairs having an area which, when viewed from outwardly of the substrate from a point on such etch axes, approximates a parallelogram which is bounded at a plurality of its corners by individual bit line contacts.

35. A method of forming a plurality of DRAM capacitors comprising:

etching capacitor container openings for an array in a substrate in at least two separate etching steps, and forming electrically insulative partitions between adjacent capacitors intermediate the two etching steps.

36. The method of claim 35 wherein the forming electrically insulative partitions step comprises:

forming insulative material over the substrate; and

conducting an anisotropic etch of the insulative material to a degree sufficient to leave the partitions.

37. A processing method of forming a plurality of DRAM capacitors comprising etching capacitor container openings for a capacitor array in a substrate in two separate etching steps.

38. A DRAM capacitor array comprising:

a plurality of 6-capacitor geometries over a substrate, individual 6-capacitor geometries being defined by a plurality of individual generally polygonal capacitor geometries, and

further, individual 6-capacitor geometries, when viewed from above the substrate, approximating a hexagon, each individual side of which being defined by a side of a different respective one of the individual polygonal capacitor geometries.

39. The DRAM capacitor array of claim 38, wherein individual polygonal capacitor geometries, when viewed from above the substrate approximate a wedge shape.

40. The DRAM capacitor array of claim 38, wherein individual polygonal capacitor geometries, when viewed from above the substrate approximate a triangle.

41. The DRAM capacitor array of claim 38, wherein individual polygonal capacitor geometries, when viewed from above the substrate approximate an isosceles triangle.

42. The DRAM capacitor array of claim 38, wherein individual polygonal capacitor geometries, when viewed from above the substrate approximate an isosceles triangle equal adjacent angles of which approximate a range of between about 50° to 70°.

43. The DRAM capacitor array of claim 38, wherein individual polygonal capacitor geometries, when viewed from above the substrate approximate an isosceles triangle equal adjacent angles of which approximate about 65°.

44. The DRAM capacitor array of claim 38, wherein the hexagon can be bisected into halves containing exactly three individual polygonal capacitor geometries.

45. A DRAM capacitor array comprising:

a plurality of 3-capacitor geometries over a substrate, individual 3-capacitor geometries, when viewed from above the substrate being defined by a pair of overlapping approximated parallelograms, the intersection of which approximates a triangle.

46. A method of forming adjacent devices over a substrate comprising:

lithographically forming an array of patterned device outlines over a substrate, the outlines defining alternating male/female patterns;

forming electrically insulative sidewall spacers in the female patterns;

after forming the electrically insulative sidewall spacers, removing the male patterns; and

after removing the male patterns, forming circuit devices adjacent the spacers.

47. An integrated device array of substantially identically shaped devices comprising:

a plurality of spaced upstanding anisotropically etched electrically insulative spacers; and

a plurality of devices formed over the substrate intermediate the spacers with the spacers being positioned intermediate adjacent devices, adjacent devices having a pitch which is substantially no greater than about the distance between a pair of adjacent spacers plus the width of the spacer between the adjacent devices.

48. The integrated device array of claim 47, wherein the devices are conductive lines.

49. The integrated device array of claim 47, wherein the devices are capacitors.

50. The integrated device array of claim 47, wherein the devices are capacitors and the device array forms part of a DRAM device.

ABSTRACT OF THE DISCLOSURE

Semiconductor processing methods include forming a plurality of patterned device outlines over a semiconductor substrate, forming electrically insulative partitions or spacers on at least a portion of the patterned device outlines, and forming a plurality of substantially identically shaped devices relative to the patterned device outlines. Individual formed devices are spaced from at least one other of the devices by a distance no more than a width of one of the electrically insulative spacers. In such manner, device pitch is reduced by almost fifty percent. According to one aspect, elongated electrically conductive lines are formed. According to another aspect, capacitors are formed which, according to a preferred embodiment form part of a dynamic random access memory (DRAM) array.

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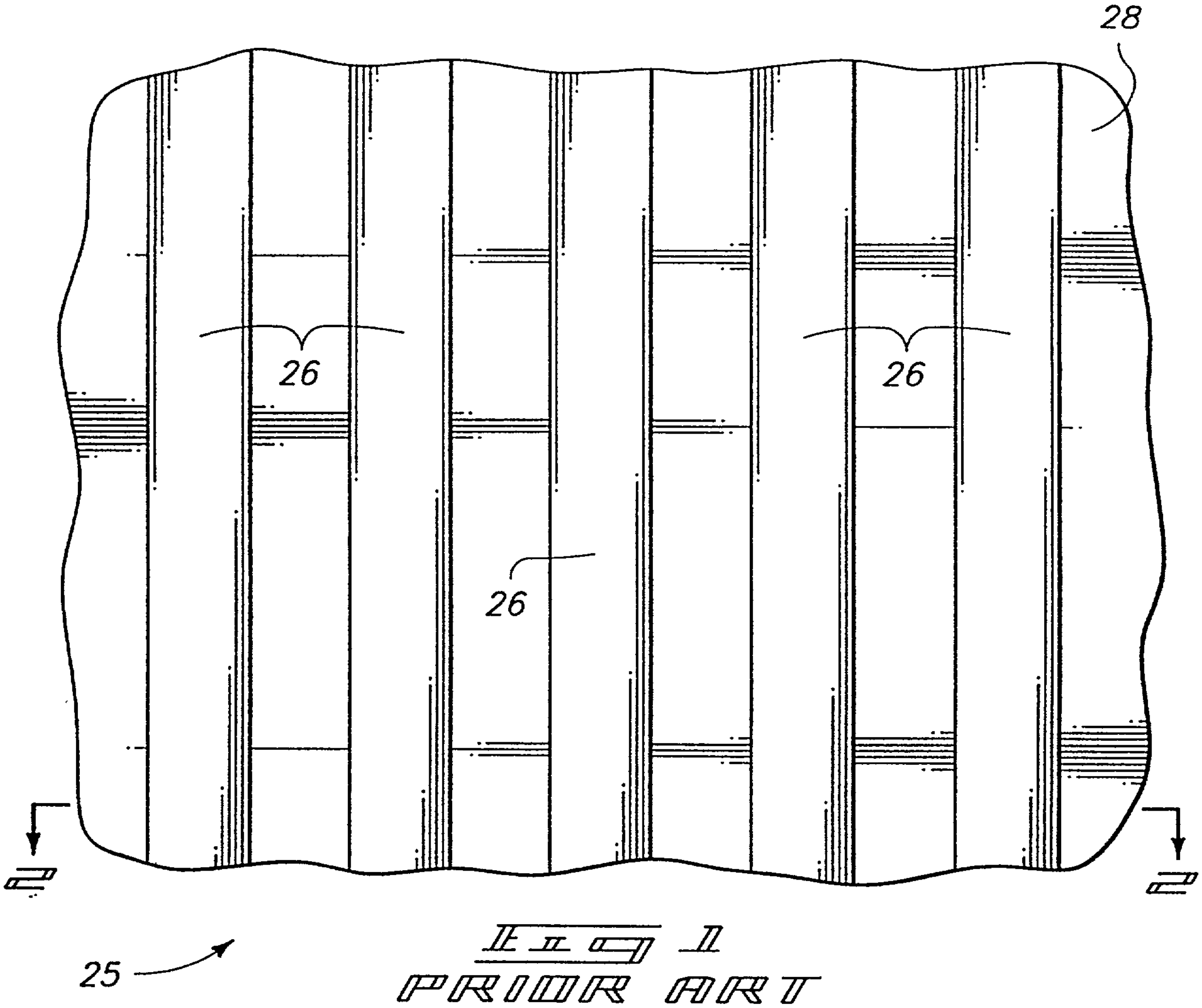

Fig 1
PRIOR ART

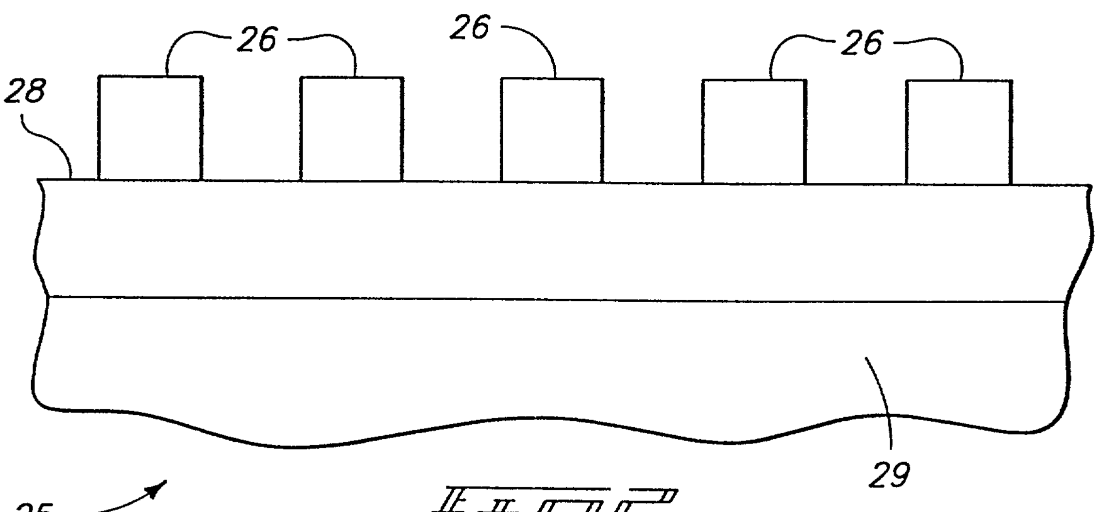

Fig 2
PRIOR ART

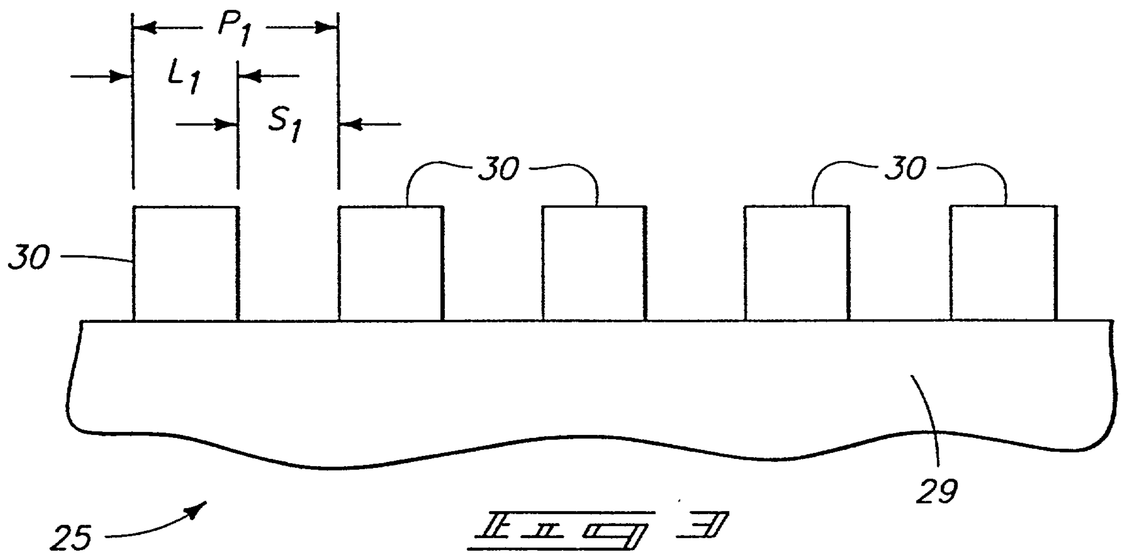

FIG 3
PRIOR ART

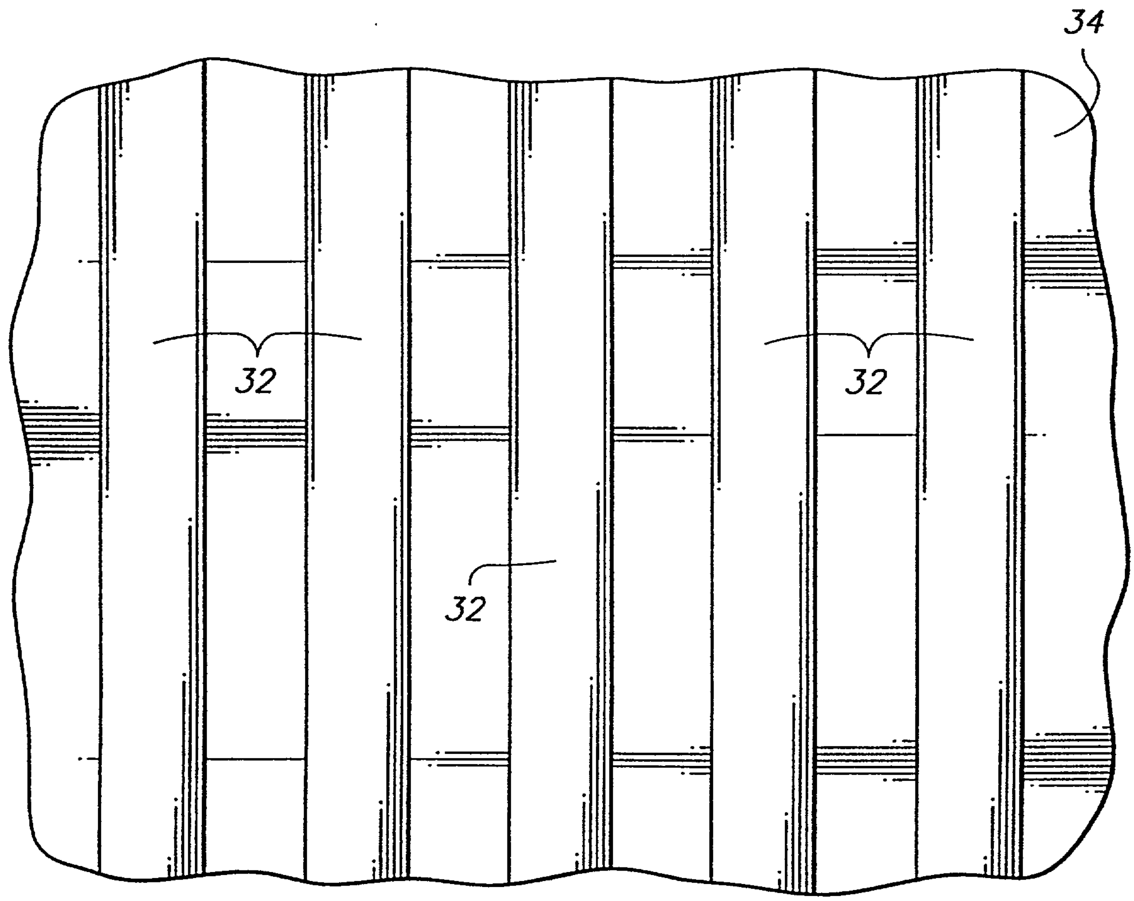

FIG 4

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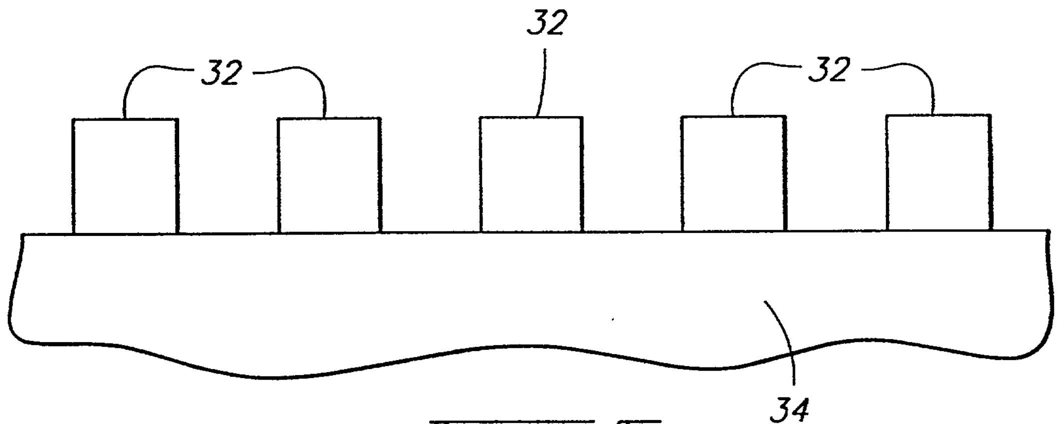

Fig 5

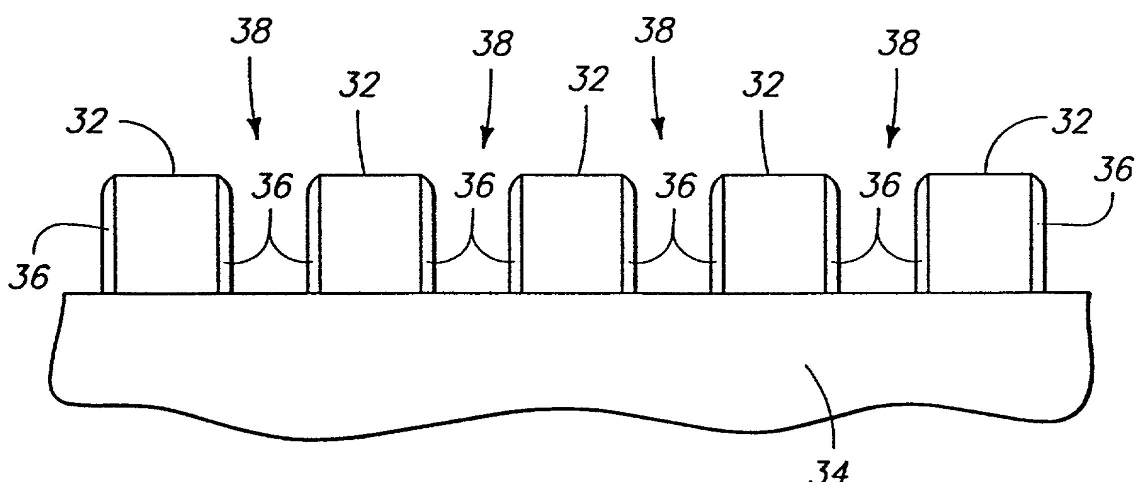

Fig 6

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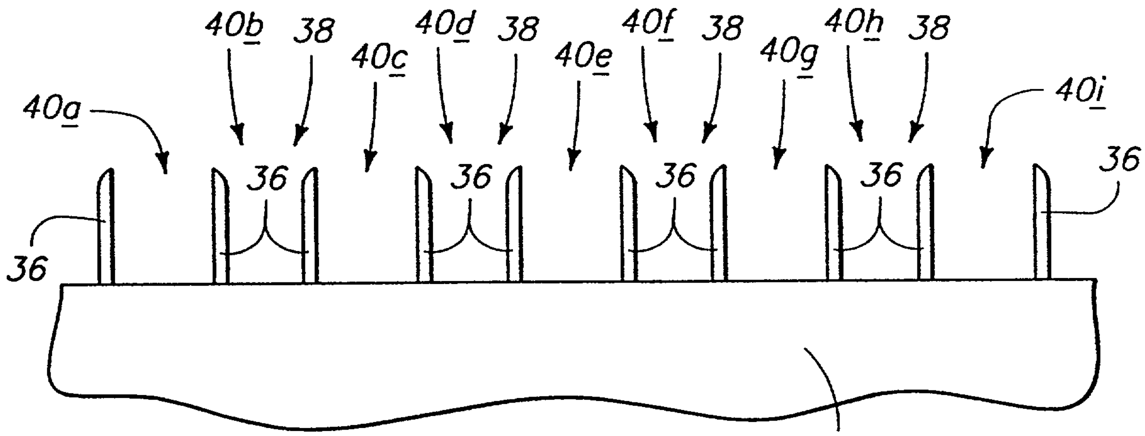

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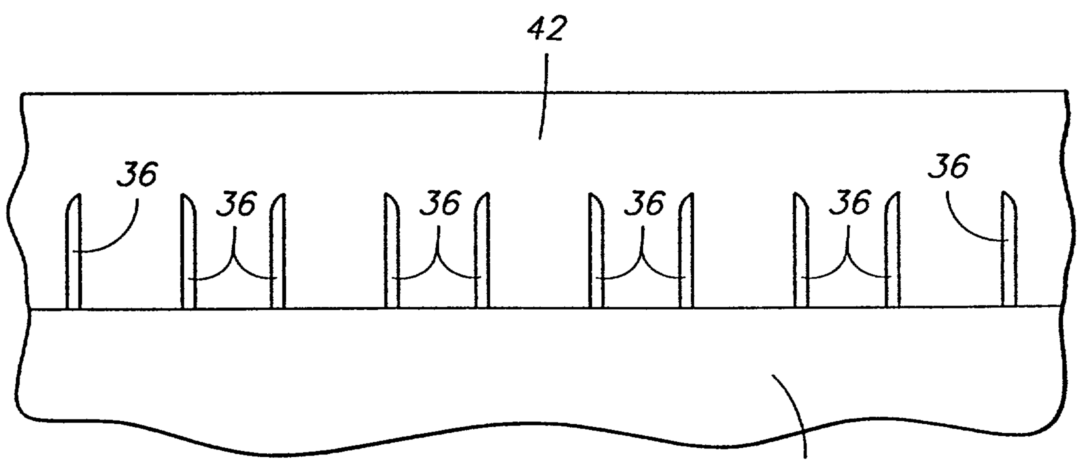

Fig 8

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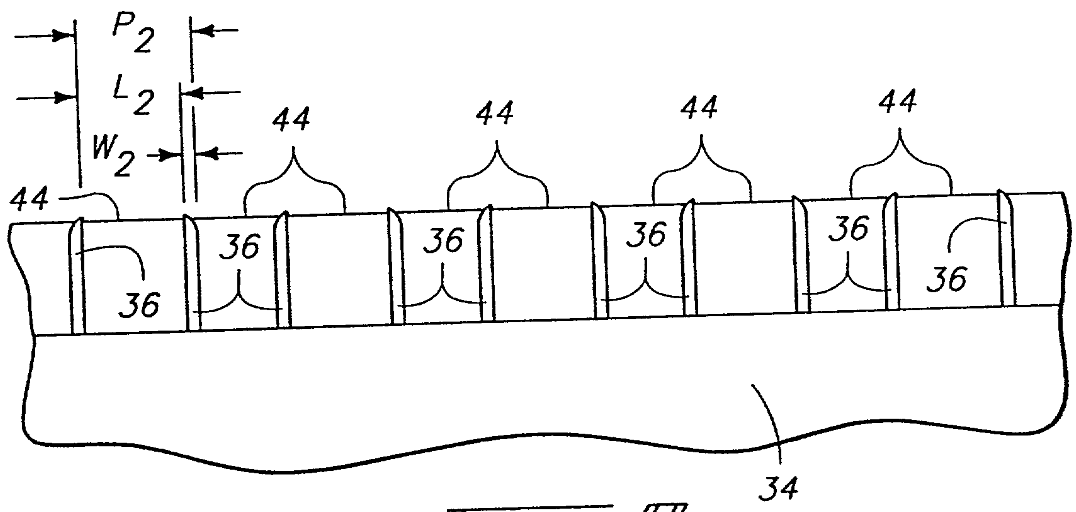

FIG 9

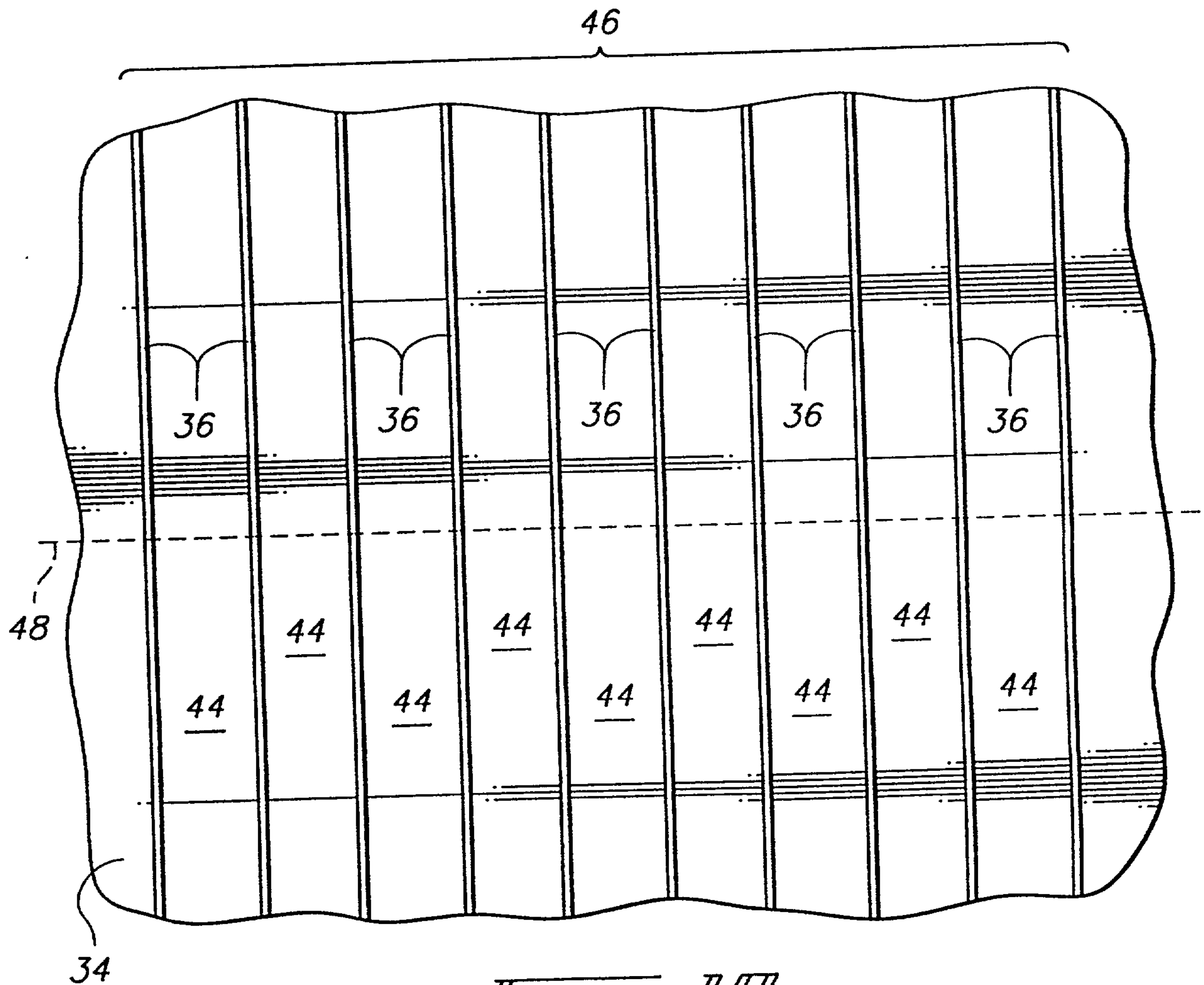

FIG 10

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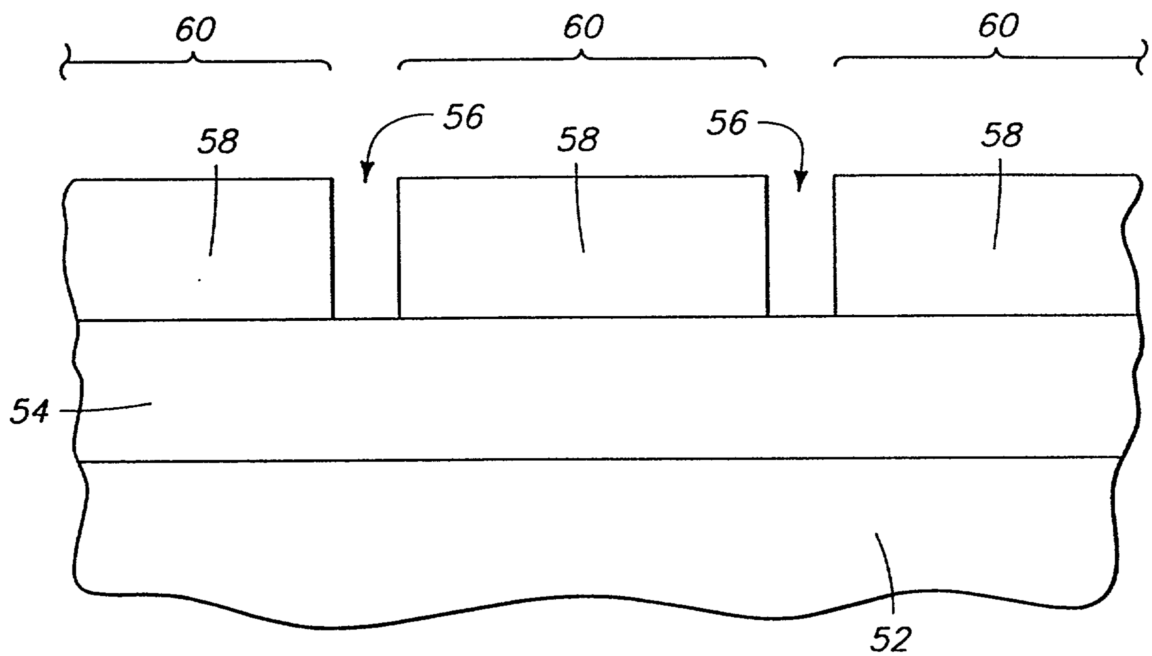

Fig. 11

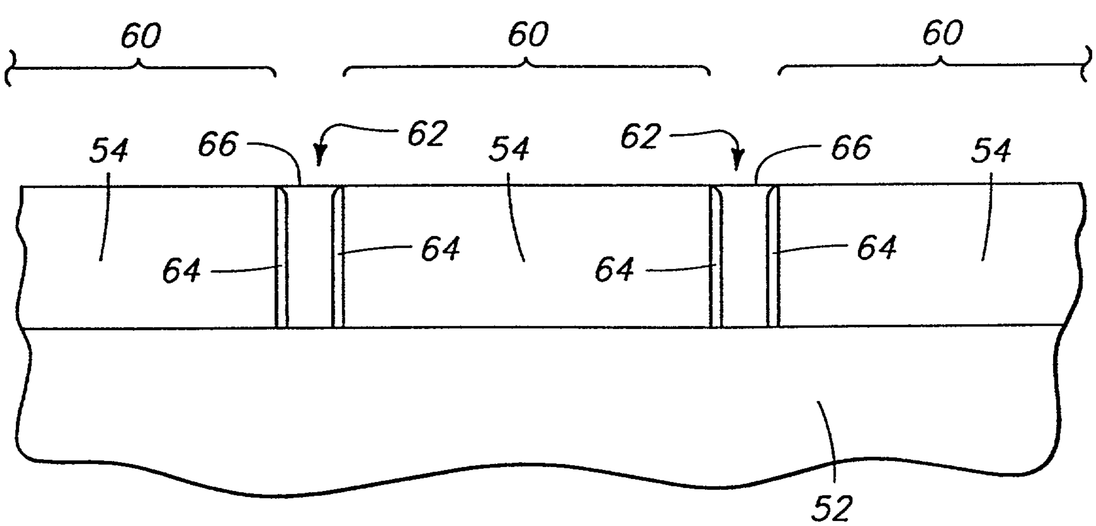

Fig. 12

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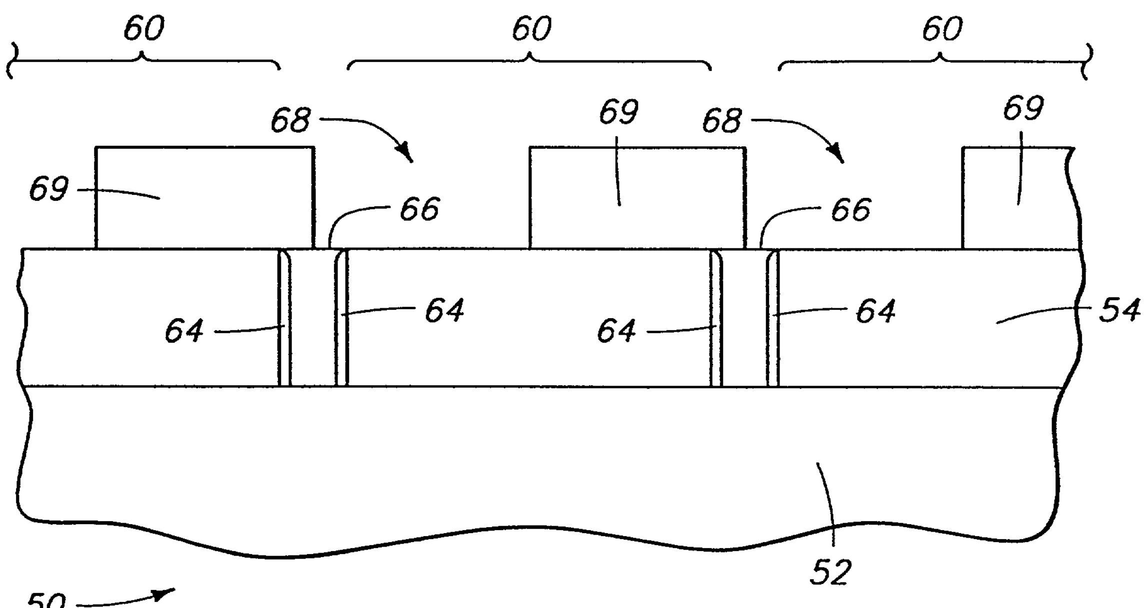

Fig. 13

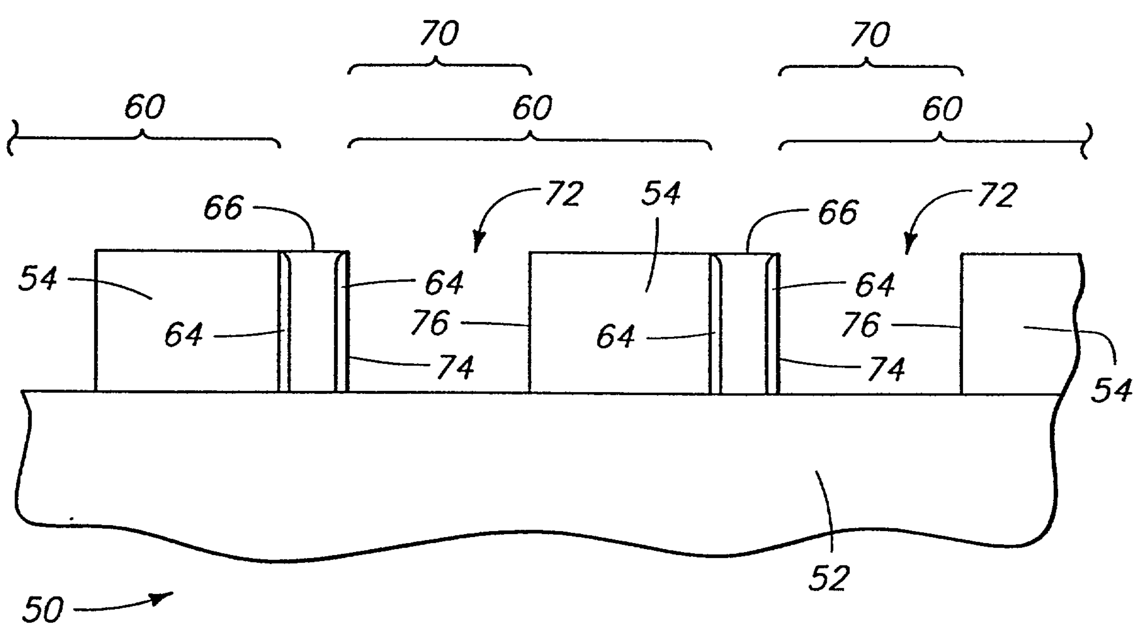

Fig. 14

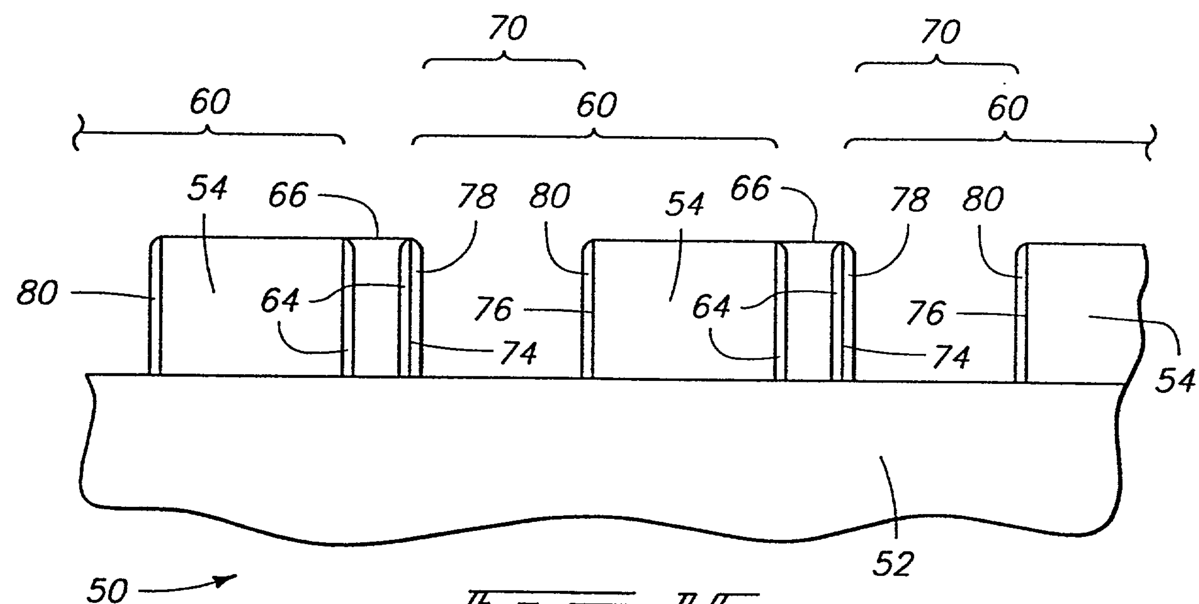
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Fig 15

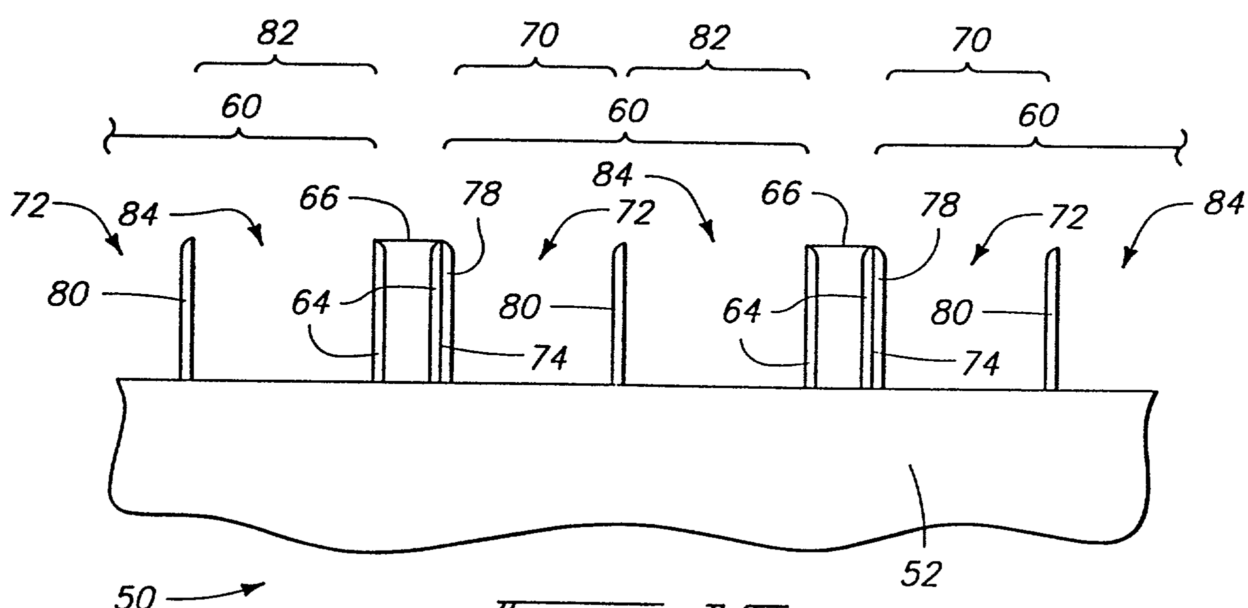
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Fig 16

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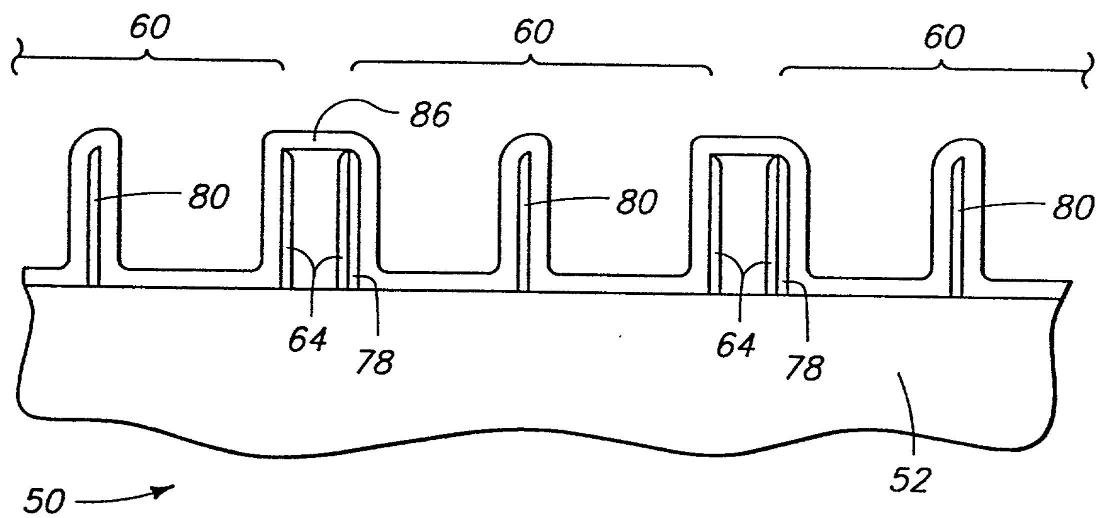

Fig. 17

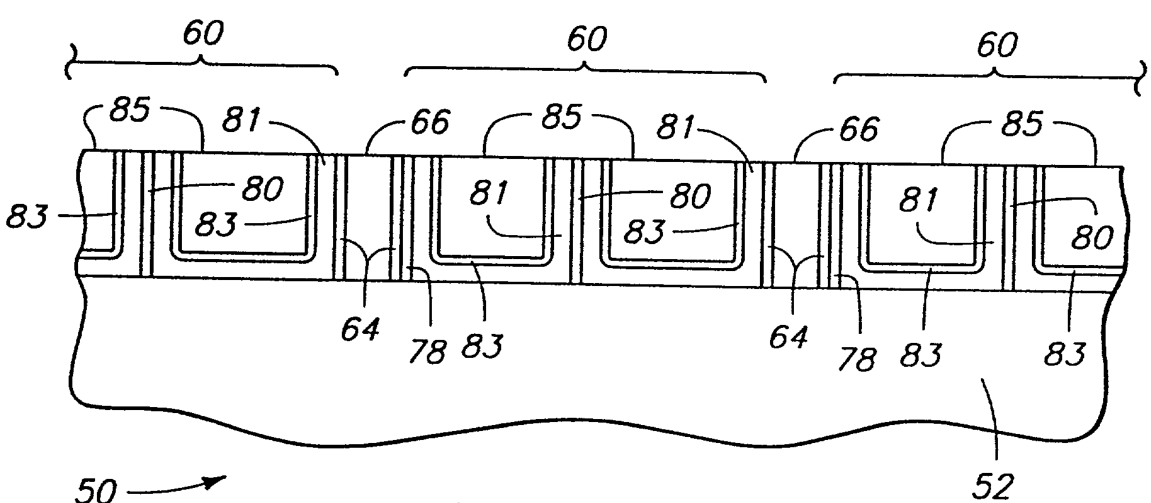

Fig. 18

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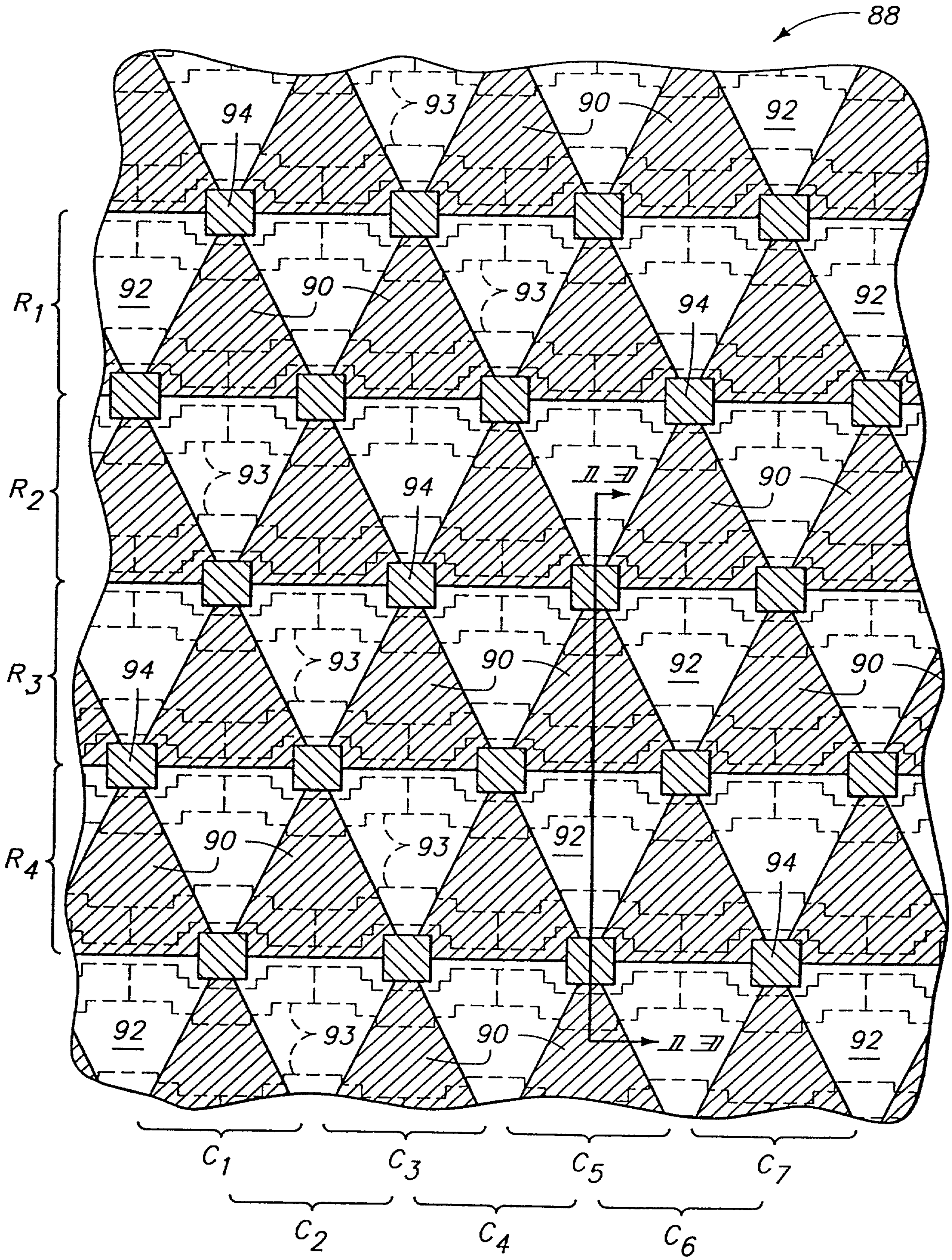

FIG 19

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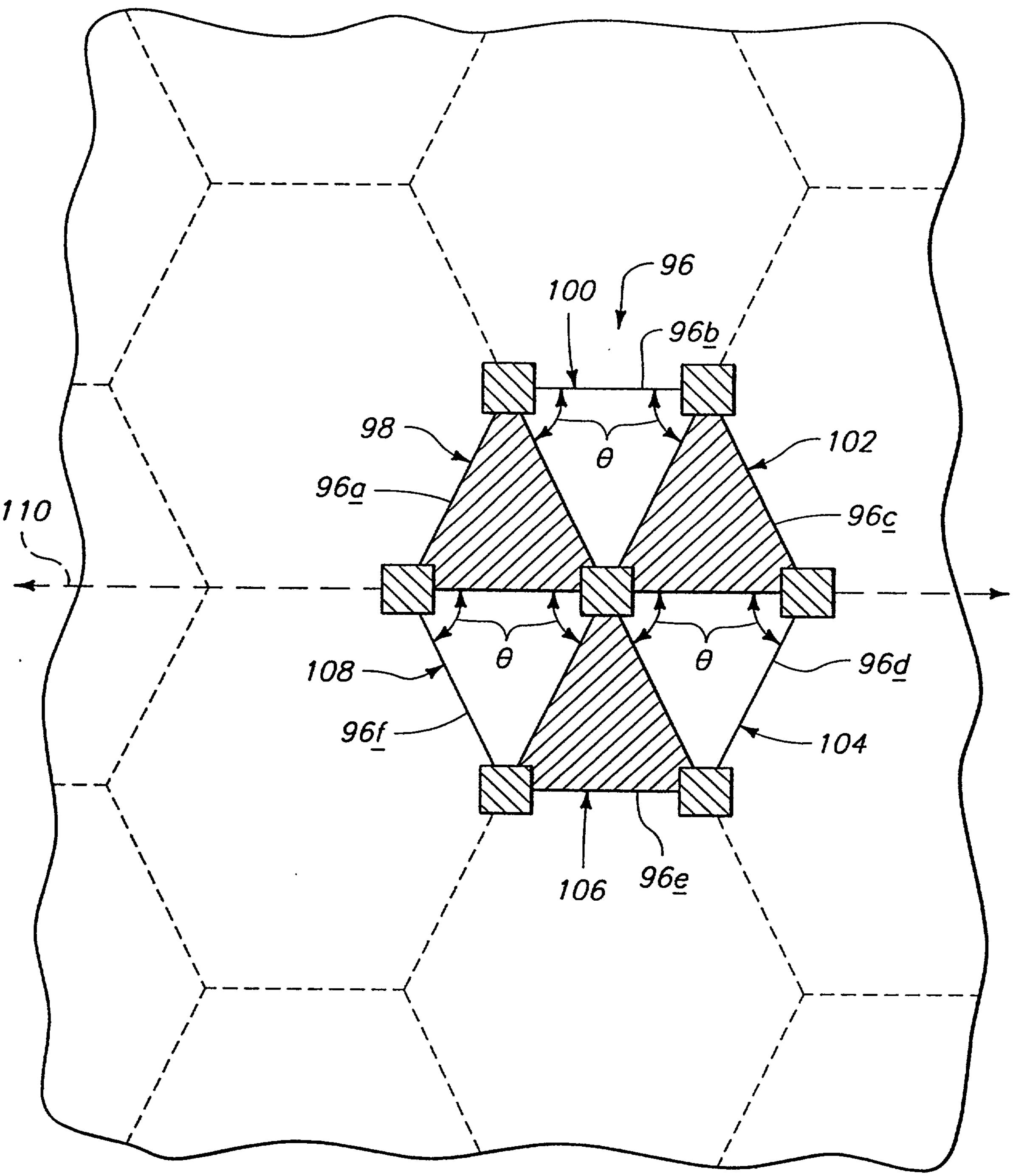

Fig 20

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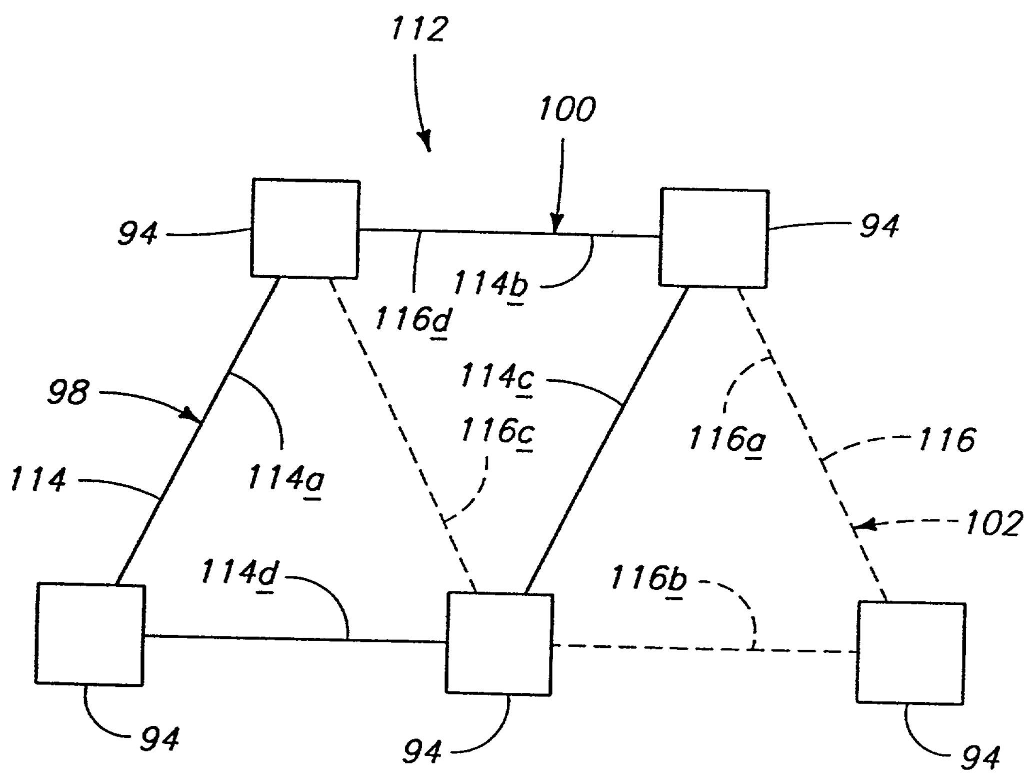

Fig 21

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DECLARATION OF SOLE INVENTOR FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Semiconductor Processing Methods of Forming Devices on a Substrate, Forming Device Arrays on a Substrate, Forming Conductive Lines on a Substrate, and Forming Capacitor Arrays on a Substrate, and Integrated Circuitry, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

EM156306369

POWER OF ATTORNEY:

As a named Inventor, I hereby appoint the following attorneys and agent to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Richard J. St. John, Reg. No. 19,363; David P. Roberts, Reg. No. 23,032; Randy A. Gregory, Reg. No. 30,386; Mark S. Matkin, Reg. No. 32,268; James L. Price, Reg. No. 27,376; Deepak Malhotra, Reg. No. 33,560; Mark W. Hendricksen, Reg. No. 32,356; David G. Latwesen, Reg. No. 38,533; George G. Grigel, Reg. No. 31,166; Keith D. Grzelak, Reg. No. 37,144; John S. Reid, Reg. No. 36,369; Lance R. Sadler, Reg. No. 38,605; James D. Shaurette, Reg. No. 39,833; W. Bryan Farney, Reg. No. 32,651; Lia M. Pappas, Reg. No. 34,095; and Michael L. Lynch, Reg. No. 30,871.

Send correspondence to: WELLS, ST. JOHN, ROBERTS, GREGORY & MATKIN P.S., 601 W. First Avenue, Suite 1300, Spokane, WA 99204-0317. Direct telephone calls to: Lance R. Sadler (509) 624-4276.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under

Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * *

Full name of sole inventor: **Werner Juengling**

Inventor's Signature: Werner Juengling

Date: 23-OCT-96

Residence: **Boise, Idaho**

Citizenship: **Austria / Europe**

Post Office Address: **5660 S. Tecoma Place**
Boise, ID 83705